



## Introduction to DSP

### Programming a DSP processor: MIPS, MOPS and

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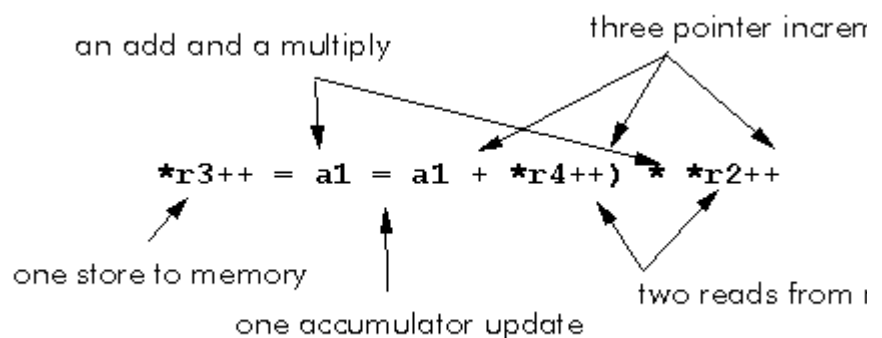
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The development of efficient assembly language code shows how a processor can be: each assembler instruction is performing several operations. But it also shows how difficult it can be to program such a specialised processor efficiently.

```
temp = *c_ptr++) * *x_ptr--);
a1 = *r3++ * *r4--
for (k = 1; k < N-1; k++)
do 0,r1
temp = temp + *c_ptr++ * *x_ptr--
a1 = a1 + *r3++ * *r4--
*y_ptr++ = temp
*r2++ = a1
```

Bear in mind that we use DSP processors to do specialised jobs fast then it may be permissible to throw away processor power by inefficiency. In that case we would perhaps be better advised to choose an easier processor in the first place. A sensible reason to use a DSP processor is to perform operations at the lowest cost, or at highest speed. In either case, wasting processor power for more hardware which makes a more expensive system which leads to an expensive final product which, in a sane world, would lead to loss of a competitive product that was better designed.

One example shows how essential it is to make sure a DSP processor is used efficiently:



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- two arithmetic operations (an add and a multiply)
- three memory accesses (two reads and a write)
- one floating point register update

- three address pointer increments

All of these operations can be done in one instruction. This is how it is made fast. But if we don't use any of these operations, we are throwing away the potential of the processor and may be slowing it down drastically. One instruction can be translated into MIPS or Mflops.

The processor runs with an 80 MHz clock. But, to achieve four memory accesses per instruction it uses a [modified von Neuman](#) memory architecture which divides the system clock by four, resulting in an instruction rate of 20 MOPS. In manic marketing mode, we can have fun working out ever higher MOPS ratings as follows:

### 80 MHz clock

20 MIPS = 20 MOPS

but 2 floating point operators per cycle = 40 MOPS

and four memory accesses per instruction = 80 MOPS

plus three pointer increments per instruction = 60 MOPS

plus one floating point register update = 20 MOPS

making a grand total MOPS rating of 200 MOPS

Which exercise serves to illustrate three things:

- MIPS, MOPS and Mflops are misleading measures of DSP power
- marketing men can squeeze astonishing figures out of nothing

Of course, we omitted to include in the MOPS rating (as some marketing man might see the possibility of DMA on [serial port](#) and [parallel port](#), and all those associated DMA address pointers, and if we had multiple [comm ports](#), each with its own DMA, really wild...

Apart from a cheap laugh at the expense of marketing, there is a valuable lesson to be drawn from this exercise. Suppose we only did adds with this processor. Its Mflops rating falls from a respectable 40 Mflops to a pitiful 20 Mflops. If we omit the memory accesses, or the pointer increments, then we can cut the MOPS rating from 200 MOPS to 20 MOPS.

It is very easy indeed to write very inefficient DSP code. Luckily it is also very easy, with a little care, to write very efficient DSP code.

